Amendments to the Claims

1. (*Currently Amended*) A detector for detecting a differential binary signal having a first signal level during a first period and a second signal level during a second period, the detector comprising:

~~[[-]]~~ an amplitude detection circuit for producing an amplitude signal indicative of the amplitude of both the first and the second period of the binary signal,

~~[[-]]~~ a slice level detection circuit for producing a slice level signal indicative of the average slice level to be applied to the binary signal,

~~[[-]]~~ an output circuit for outputting the detected binary signal,

~~[[-]]~~ an offset circuit for producing a slice level offset signal in response to the outputted binary signal, the slice level signal and the amplitude signal, and

~~[[-]]~~ a level shift circuit coupled to the output circuit ~~(4)~~ for level shifting the binary signal in response to the slice level offset signal,

wherein said circuits are coupled so as to detect the differential binary signal using a first slice level during the first period and using a second slice level during the second period, and wherein all said circuits are differential circuits.

2. (*Original*) A detector according to claim 1, wherein the output circuit comprises a limiter circuit.

3. (*Currently Amended*) A detector ~~according to claim 1 or 2,~~ according to claim 1, further comprising a first additional level shift circuit coupled to the amplitude detection circuit and/or a second additional level shift circuit coupled to the slice level detection circuit.

4. (*Currently Amended*) A detector ~~according to any of the preceding claims,~~ according to claim 1, further comprising a decoupling circuit for decoupling the binary signal prior to feeding it to the other circuits.

5. (*Currently Amended*) An offset circuit for use in a detector ~~according to any of the preceding claims,~~ according to claim 1, the offset circuit comprising:

~~[[ ]]~~ a first differential amplifier for processing the detected differential binary signal, and

~~[[ ]]~~ at least a second differential amplifier for processing the slice level signal and its inverse.

6. (*Currently Amended*) An offset circuit ~~according to claim 5 or 6,~~ according to claim 5, wherein the slice level offset signal is limited to a maximum and a minimum value.